VERIFICATION OF TRANSLATION

I, Woo-Hyun WHANG, of Suite 1810, Hwanghwa Bldg., 832-7, Yeoksam-dong, Gangnam-gu, Seoul, Republic of Korea hereby declare that I am knowledgeable in the English and Koean languages, and that to the best of my knowledge the attached document is a true and complete English translation of Korean Patent Application No. 10-2003-0049076.

Dated August 4, 2006

Woo-Hyun Hwang

Signature

Translation of Priority Document

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[Abstract of the Disclosure]

[Abstract]

A high-speed flat panel display having a long lifespan is provided. The high-speed flat panel display has thin film transistors with different geometric structures in a pixel part in which a plurality of pixels are arranged, and a driving circuit part for driving the pixels.

The flat panel display includes: a pixel part in which a plurality of pixels are arranged; and a driving circuit part for driving the pixels in the pixel part, in which thin film transistors constituting the pixel part and the driving circuit part have different geometric structures in a gate or drain region.

One of the thin film transistors driving the pixel part and the thin film transistors constituting the driving circuit part has a zigzag-shaped gate or drain region, or is equal in length and narrower, equal in width and longer, or narrower and longer than other thin film transistors.

[Typical Figure]

FIG. 3B

[Specification]

[Title of the Invention]

FLAT PANEL DISPLAY

[Brief Description of the Drawings]

FIG. 1 illustrates the structure of a conventional organic light emitting display;

FIG. 2 is a plan view illustrating a thin film transistor of a driving circuit part in an organic light emitting display according to an exemplary embodiment of the invention;

FIGS. 3A and 3B are plan and cross-sectional views illustrating a thin film transistor of a pixel part in an organic light emitting display according to a first exemplary embodiment of the invention;

FIGS. 4A and 4B are plan and cross-sectional views illustrating a thin film transistor of a pixel region in an organic light emitting display according to a second exemplary embodiment of the invention; and

FIG. 5 is a plan view illustrating a thin film transistor of a pixel part in an organic light emitting display according to a third exemplary embodiment of the invention.

* Explanation of the signs that are the main part of the drawings

220, 320, 420, 520: semiconductor layer

240, 340, 440, 540: gate

221, 225, 321, 325, 421, 425, 521, 525: source and drain

regions

251, 255, 351, 355, 451, 455, 551, 555: source and drain contacts

261, 265, 361, 365, 461, 465, 561, 565: source and drain electrodes

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a full-color flat panel display, and more particularly, to a high-speed flat panel display with a long lifespan which has thin film transistors formed in different geometric structures in a pixel part and a driving circuit part.

In general, an organic light emitting display, a flat panel display, includes a pixel part 110 in which a plurality of pixels are arranged in a matrix form on an insulating substrate 100, and a driving circuit part for driving the pixel part 110 as shown in FIG. 1. The pixel part 100 is not shown in the figure but has multiple gate lines, multiple data lines, and multiple common power lines, and the plurality of pixels connected to these lines are arranged in a matrix form. Each pixel includes an electroluminescent (EL) device, a driving transistor for supplying driving current in response to a data signal from the data line to the EL device, a switching transistor for transmitting a data signal to the driving transistor in response to a scan signal supplied to the gate line, and a

capacitor for storing the data signals.

The driving circuit part for driving the pixels in the pixel part 110 includes a gate driving circuit part 130 for providing a scan signal enabling the gate line of the pixel part 110 to be driven, and a data driving circuit part 120 for providing a data signal to the data line of the pixel part 110.

In a conventional active matrix organic light emitting display (AMOLED), all thin film transistors which are disposed in the pixel part (100) and the driving circuit parts 120 and 130 are formed of polysilicon. In an AMOLED having a high resolution of 180 ppi or more, when the thin film transistors in the pixel and driving circuit parts are formed of polysilicon, a high-speed operation characteristic could be obtained from the driving circuit part due to high mobility of the thin film transistors. However, because of a high on-current, the amount of current flowing through the EL device of the pixel part became more than a threshold value, and thus luminance per unit area increased and the lifespan of the EL device was shortened.

Meanwhile, when the pixel part and the driving circuit part were composed of thin film transistors having low mobility in order to maintain the on-current characteristic as necessary, on-current became relatively lower and appropriate luminance was obtained. This solved the problem of shortening of the lifespan of the EL device, but precluded attainment of the high-speed operation characteristic of the

driving circuit part.

[Technical Object of the Invention]

Therefore, it is an object of the invention to provide a flat panel display having a long lifespan.

It is another object of the invention to provide a flat panel display in which thin film transistors disposed in a pixel part and a driving circuit part have different geometric structures enabling attainment of a high-speed operation characteristic and a long lifespan.

It is still another object of the invention to provide a flat panel display in which thin film transistors disposed in a pixel part and a driving circuit part have gate and drain regions with different shapes enabling attainment of a high-speed operation characteristic and a long lifespan.

[Construction of the Invention]

One aspect of the invention provides a flat panel display including a pixel part in which a plurality of pixels are arranged and a driving circuit part for driving the pixels of the pixel part. Thin film transistors constituting the pixel and driving circuit parts have different geometric structures in a gate region.

One of the thin film transistors driving the pixel part and the thin film transistors constituting the driving circuit part may have a zigzag-shaped gate region. Or, it may be equal in length and narrower, equal in width and longer, or narrower and longer than other thin film

transistors.

The thin film transistor with a different shape may include multiple gates, and a high resistance offset region may be included between the multiple gates. The offset region may have a zigzag shape or be longer or narrower than other thin film transistors.

Another aspect of the invention provides a flat panel display including: a pixel part in which a plurality of pixels are arranged; and a driving circuit part for driving the pixels of the pixel part. Thin film transistors constituting the pixel and driving circuit parts provide a flat panel display having different geometric structures at least in a drain region.

One of the thin film transistors driving the pixel part and the thin film transistors constituting the driving circuit part may have a zigzag-shaped drain region. Or, it may be equal in length and narrower, equal in width and longer, or narrower and longer than other thin film transistors.

The thin film transistor with a different shape may at least have a drain region with a high resistance offset region. The drain offset region may have a zigzag shape, or be longer or narrower than in other thin film transistors.

Still another aspect of the invention provides a flat panel display including: a pixel part in which a plurality of pixels are arranged; and gate and data driving circuit parts for driving the pixels of the pixel part.

At least one of thin film transistors constituting the pixel part has a different geometric structure from at least one of thin film transistors constituting the gate and data driving circuit parts.

At least one of the thin film transistors constituting the pixel part may include an offset region in a gate or drain region. The offset region may have a zigzag shape, or be longer or narrower than the thin film transistors constituting the gate or data driving circuit part.

The present invention will now be described more fully hereinafter with reference to the attached drawings, wherein the same numerals denote the same components.

FIG. 2 is a plan view illustrating a thin film transistor constituting a circuit part in an organic light emitting display of the invention.

Referring to FIG. 2, the thin film transistor constituting the pixel part includes a semiconductor layer 220 formed of polysilicon, a gate electrode 240, and source and drain electrodes 261 and 265. The semiconductor layer 220 includes a channel region 224 corresponding to the gate electrode 240, and source and drain regions 221 and 225 formed at both sides of the channel region 224. The source and drain electrodes 261 and 265 are electrically connected to the source and drain regions 221 and 225 through contacts 251 and 255.

FIGS. 3A and 3B illustrate a first example of a thin film transistor constituting a gate or data driving circuit part in an organic light emitting display according to an exemplary embodiment of the

invention. FIG. 3A is a plan view of a thin film transistor, and FIG. 3B is a cross-sectional view of a thin film transistor taken along line 3B-B' of FIG. 3A.

Referring to FIGS. 3A and 3B, the thin film transistor of the driving circuit part includes a semiconductor layer 320, a gate electrode 340, and source and drain electrodes 361 and 365. The gate electrode 340 includes multiple gates 341 and 345 corresponding to the semiconductor layer 320.

The semiconductor layer 320 has a "⊏"-shaped structure which includes multiple channel regions 323 and 327 respectively corresponding to the multiple gates 341 and 345 of the gate electrode 340, and high-concentration source and drain regions 321 and 325 formed at one side of each of the channel regions 323 and 327, respectively. Also, the semiconductor layer 320 further includes an offset region 330 interposed between the multiple channel regions 323 and 327, i.e., between the multiple gates 341 and 345. The source and drain electrodes 361 and 365 are electrically connected to the high-concentration source and drain regions 321 and 325 formed in the semiconductor layer 320 through contacts 351 and 355, respectively.

The offset region 330 has a zigzag shape and is a high resistance region which comprises a low-concentration impurity region entirely or partially doped with an impurity having the same conductivity type as the high-concentration source and drain regions 321 and 325 at

a lower concentration than the source and drain regions, or an intrinsic region not doped with any impurity.

FIGS. 4A and 4B illustrate a second example of a thin film transistor of a pixel region in an organic light emitting display according to an exemplary embodiment of the invention. FIG. 4A is a plan view of a thin film transistor, and FIG 4B is a cross-sectional view of a thin film transistor taken along line 4B-4B' of FIG. 4A.

The resistance of the thin film transistor illustrated in FIGS. 4A and 4B is changed by altering a shape of an offset region between multiple gates as in the first example of FIGS. 3A and 3B.

That is, the thin film transistor of the pixel part includes a "⊏"-shaped semiconductor layer 420, a gate electrode 440, and source and drain electrodes 461 and 465. The gate electrode 440 includes multiple gates 441 and 445 corresponding to the semiconductor layer 420. The source and drain electrodes 461 and 465 are electrically connected to high-concentration source and drain regions 421 and 425 of the semiconductor layer 420 through contacts 451 and 455, respectively.

The semiconductor layer 420 includes multiple channel regions 423 and 427 respectively corresponding to the multiple gates 441 and 445 of the gate electrode 440, and the high-concentration source and drain regions 421 and 425 formed at one side of each of the multiple channel regions 423 and 427, respectively. Also, the semiconductor

layer 420 includes an offset region 430 interposed between the multiple gates 441 and 445, i.e., the multiple channel regions 423 and 427.

The shape of the offset region 430 is altered to be narrower than a conventional offset region, and thus the offset region 430 has relatively large resistance. The offset region 430 is a high resistance region which comprises a low-concentration impurity region doped with an impurity having the same conductivity type as the high-concentration source and drain regions 321 and 325 at a lower concentration than the source and drain regions421 and 425, or an intrinsic region not doped with any impurity.

There are methods for altering a shape of an offset region like the thin film transistor of the second example, which include: maintaining a certain length (Ld) and decreasing a width (Wd), maintaining a certain width (Wd) and increasing a length (Ld), and decreasing a width (Wd) and increasing a length (Ld). This alters a size (Wd/Ld) of the offset region 430 and thus enables the resistance thereof to be changed.

Referring to the first and second examples, when the thin film transistor of the pixel part forms the offset region between the multiple gates, and the shape of the offset region is altered in zigzag or its size is changed, resistance increases. Thus, when the driving circuit part is composed of the thin film transistor illustrated in FIG. 2, and the pixel part is composed of the thin film transistor with a high resistance offset

region interposed between the multiple gates, illustrated in FIGS. 3A, 3B, 4A and 4B, the driving circuit part maintains a high-speed operation characteristic as in a conventional organic light emitting display, and the pixel part reduces the current flowing through the EL device due to an increase in the resistance of the thin film transistor. Accordingly, the lifespan of the display may be extended.

That is, when the gate regions in the thin film transistor of the pixel part in the first and second examples are set to be a multi-channel region under the multi gates and an offset region between the multi gates, and the gate region in the thin film transistor of the driving circuit part illustrated in FIG. 2 is set to be a channel region under the gates, the gate region in the thin film transistor of the driving circuit part may maintain the high-speed operation characteristic because of the small resistance as in the conventional thin film transistor. Meanwhile, the gate region in the thin film transistor of the pixel part has a large resistance as the shape of the offset region is altered, and thus the current flowing through the EL device may be controlled and appropriate luminance may be generated, thereby extending the device's lifespan.

FIG. 5 is a plan view illustrating a third example of a thin film transistor of a pixel part in an organic light emitting display according to an exemplary embodiment of the invention.

Referring to FIG. 5, the thin film transistor constituting the pixel

part includes a semiconductor layer 520 formed of polysilicon, a gate electrode 540, and source and drain electrodes 561 and 565. The semiconductor layer 520 includes a channel region 524 corresponding to the gate electrode 540, and source and drain regions 521 and 525 formed at both sides of the channel region 524. The source and drain electrodes 561 and 565 are electrically connected to the source and drain regions 521 and 525 through contacts 551 and 555, respectively.

The semiconductor layer 520 further includes an offset region 527 between the channel region 524 and the drain region 525. The offset region 527 has a zigzag shape. Like in the thin film transistor of the third example, there are other methods for altering the shape of a drain offset region, which include: maintaining the length of the drain region constant and decreasing the width of the drain region, maintaining the width constant and increasing the length, and reducing the width and increasing the length, thereby altering the size of the offset region 527.

According to the third example, though it is illustrated that the thin film transistor of the pixel part includes the offset region 527 only in the drain region 525, both the source and drain regions 521 and 525 may have offset regions therein.

According to the third example, the thin film transistor of the pixel part has the offset region 527 in the drain region 525, and thus resistance increases. Accordingly, when the driving circuit part is

composed of the thin film transistor as illustrated in FIG. 2, and the pixel part is composed of the thin film transistor having the drain offset region as illustrated in FIG. 5, the driving circuit part may maintain a high-speed operation characteristic like a conventional organic light emitting display, and the pixel part may reduce current flowing through the EL device due to an increase in the resistance of the thin film transistor, thereby extending the display's lifespan.

That is, since the thin film transistor of the pixel part according to the third example alters the shape of the drain offset region so as to change the resistance of the drain region, the thin film transistor of the driving circuit part has small resistance in the drain region, like a conventional thin film transistor, and thus a high-speed operation characteristic is maintained. And, the thin film transistor of the pixel part has large resistance in the drain region, thereby controlling current flowing through the EL device and generating appropriate luminance, and thus the device's lifespan may be extended.

In the exemplary embodiments of the invention, while a thin film transistor of a pixel part has a high resistance offset region between multiple gates or in a drain region, so as to change the resistance of the thin film transistor in the pixel part depending on a doping state of the offset region and control current flowing through the EL device, the offset region may be formed in all thin film transistors constituting a pixel region or only in a corresponding thin film transistor.

A high resistance offset region according to the exemplary embodiments of the invention may be applied in all thin film transistors constituting a pixel part, or in at least one thin film transistor, for example, a thin film transistor for driving the EL device.

Though in the exemplary embodiments of the invention illustrated herein, the semiconductor layer has a "ㄷ"-shaped structure and the gate electrode has a dual gate, the semiconductor layer and gate can have any structure that allows the resistance of the thin film transistor in the pixel part to be changed.

[Effects of the Invention]

According to the exemplary embodiment of the invention, the shape of a gate or drain offset region of a thin film transistor of a pixel part is altered so as to change resistance in a gate or drain region, and thus a high-speed operation characteristic may be obtained and a device's lifespan may be extended.

Although the invention has been described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the invention without departing from the spirit or scope of the invention.

[Claims]

[Claim 1]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

a driving circuit part driving the pixels of the pixel part,

wherein thin film transistors constituting the pixel and driving circuit parts have different geometric structures in a gate region.

[Claim 2]

The flat panel display according to claim 1, wherein one of the thin film transistors driving the pixel part and constituting the driving circuit part has a zigzag-shaped gate region.

[Claim 3]

The flat panel display according to claim 1, wherein the gate region in the one of the thin film transistors driving the pixel part and constituting the driving circuit part is equal in length and narrower, equal in width and longer, or narrower and longer than other thin film transistors.

[Claim 4]

The flat panel display according to claim 2 or 3, wherein the one of the thin film transistors comprises multiple gates, and a high resistance offset region is disposed between the multiple gates.

[Claim 5]

The flat panel display according to claim 4, wherein the gate offset region in the one of the thin film transistors is formed in a zigzag.

[Claim 6]

The flat panel display according to claim 4, wherein the gate offset region in the one of the thin film transistors is longer or narrower than in other thin film transistors.

[Claim 7]

The flat panel display according to claim 4, wherein the one of the thin film transistors is at least one of the thin film transistors constituting the pixel part.

[Claim 8]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

a driving circuit part for driving the pixels of the pixel part,

wherein thin film transistors constituting the pixel part and the driving circuit part have different geometric structures at least in a drain region.

[Claim 9]

The flat panel display according to claim 8, wherein one of the thin film transistors driving the pixel part and constituting the driving circuit part has a zigzag-shaped drain region.

[Claim 10]

The flat panel display according to claim 8, wherein the drain

region in the one of the thin film transistors driving the pixel part and constituting the driving circuit part is equal in length and narrower, equal in width and longer, or narrower and longer than other thin film transistors.

[Claim 11]

The flat panel display according to claim 9 or 10, wherein the one of the thin film transistors has a high resistance offset region at least in a drain region.

[Claim 12]

The flat panel display according to claim 8, wherein the drain offset region in the one of the thin film transistors has a zigzag shape.

[Claim 13]

The flat panel display according to claim 8, wherein the drain offset region in the one of the thin film transistors is longer or narrower than in other thin film transistors.

[Claim 14]

The flat panel display according to claim 11, wherein the one of the thin film transistors is at least one of the thin film transistors constituting the pixel part.

[Claim 15]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

gate and data driving circuit parts for driving the pixels of the

pixel part,

wherein at least one of thin film transistors constituting the pixel part has a different geometric structure from at least one of thin film transistors constituting the gate and data driving circuit parts.

[Claim 16]

The flat panel display according to claim 15, wherein the at least one of the thin film transistors constituting the pixel part comprises an offset region in a gate or drain region.

[Claim 17]

The flat panel display according to claim 16, wherein the offset region in the at least one of the thin film transistors constituting the pixel part has a zigzag shape.

[Claim 18]

The flat panel display according to claim 16, wherein the offset region in the at least one of the thin film transistors constituting the pixel part is longer or narrower than in other thin film transistors.

FIG. 1

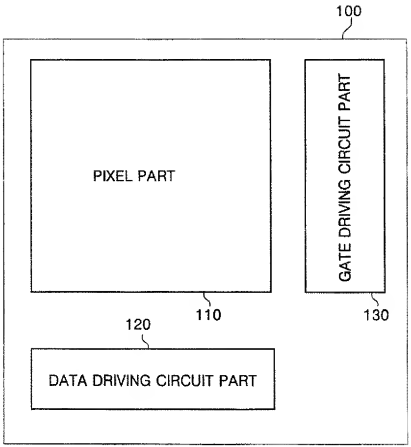

100
PIXEL PART
GATE DRIVING CIRCUIT PART
110
130
120
DATA DRIVING CIRCUIT PART

FIG. 2

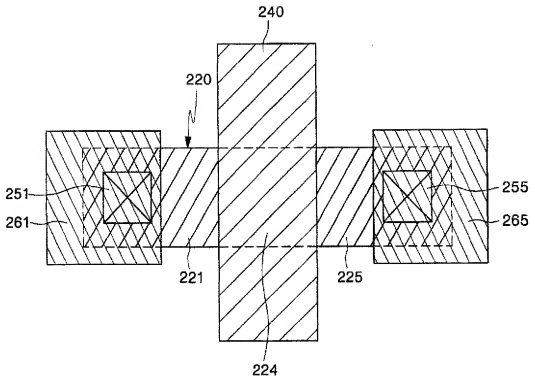


FIG. 3A

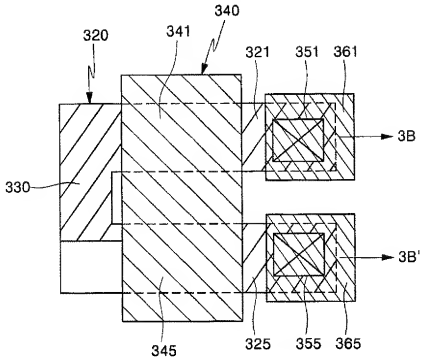

340
320
341
321
351
361
3B
330
3B'
345
325
355
365

FIG. 3B

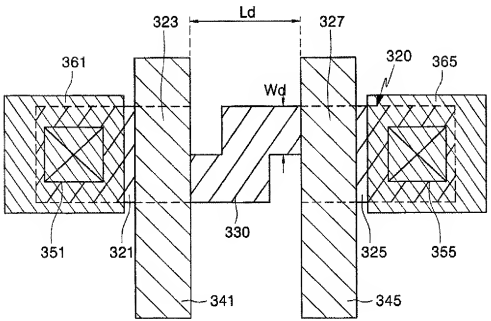
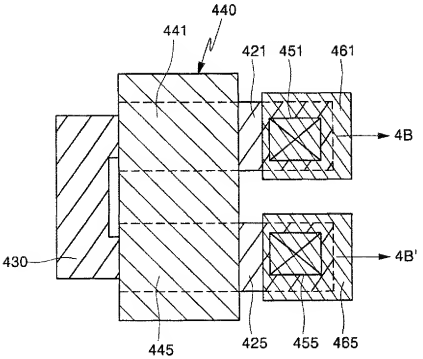

323
Ld
327
361
320
365
Wd
330
351
321
325
355
341
345

FIG. 4A


440
441
421
451
461
4B
4B'
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445
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455
465

FIG. 4B

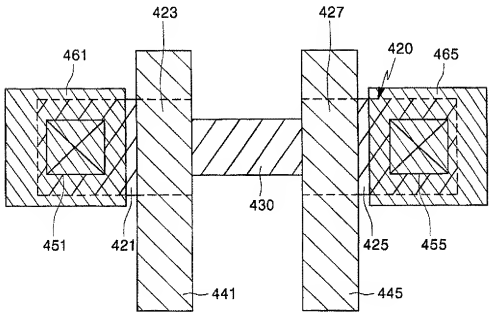
423
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FIG. 5